

CYIENT

ASIC Digital Verification Engineer Lead

募集職種

採用企業名

CYIENT株式会社

求人ID

1490820

業種

電気・電子・半導体

会社の種類

大手企業 (300名を超える従業員数)

雇用形態

正社員

勤務地

神奈川県

給与

経験考慮の上、応相談

更新日

2025年04月01日 10:00

応募必要条件

職務経験

6年以上

キャリアレベル

中途経験者レベル

英語レベル

ビジネス会話レベル

日本語レベル

ビジネス会話レベル

N2 and above

最終学歴

大学卒：学士号

現在のビザ

日本での就労許可が必要です

募集要項

Position: ASIC Digital Verification Engineer Lead

Location: Yokohama

Language: N2 and above

Job Description:

Looking for 8+ yrs of design verification Engineers with below skills

- RTL design (Verilog HDL)
- EDA verification experience (NC Verilog)
- Ability to use Microsoft Office software (Excel, Word, Outlook)
- Ability to use Linux CUI commands

- Experience with SV, UVM and SystemVerilog Assertions (SVA)
- Experience using version control tools (Subversion, git)

Knowledge that would be beneficial

- AI Insights
- Ability to check timing reports during implementation

Roles & Responsibilities

- Under general supervision, performs engineering work and applied research, development, and design of new Integrated Chips.
- Work includes Architectural Design, Logic Design, Circuit Design, Physical Design, Verification, Fabrication, Packaging of Chips

スキル・資格

会社説明