CareerCross by JAC Recruitment

Engineer/Senior Engineer Process Integration

詳細ご説明致しますので、お問い合わせください。

Job Information

Recruiter
JAC Recruitment Co., Ltd.

Hiring Company
社名非公開

Job ID
1517105

Industry
Electronics, Semiconductor

Company Type
International Company

Job Type
Permanent Full-time

Location
Hiroshima Prefecture

Salary
4.5 million yen ~ 10 million yen

Work Hours
08:30 〜 17:15

Holidays
【有給休暇】有給休暇は入社後7ヶ月目から付与されます 入社7ヶ月目には最低10日以上 【休日】完全週休二日制 年末年始 有給休…

Refreshed
April 4th, 2025 01:00

General Requirements

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Native

Minimum Education Level
Technical/Vocational College

Visa Status
Permission to work in Japan required

Job Description

【求人No NJB2238657】
As Technology Development （TD） DRAM Integration Technology department we drive next generation of DRAM memory technology development through multi functional responsibilities of module engineering materials development and device engineering in Hiroshima plant TD!

As the Engineer of Process Integration you will work well with all assigned module related development activities in Fab15

TD but also work with related MFG Process Integration modules developing process flows and process integration schemes with novel devices and new materials for next generation of DRAM as well as finding innovative and manufacturable solutions to enable a successful transitioning of the new DRAM product which is developed in Fab15 TD to the manufacturing sites.
You will ensure maximum partnership and cross・learning between the different sites and organizations.
You will also be a member of the Process R D Project team across the sites （Hiroshima Taiwan and Boise）.

■Responsibilities include but are not limited to the following:
・Project responsibilities
・Assume responsibility for all assigned module related transfer topics in F15 R D （including process flow tool selection recipe optimization characterization and data interpretation methods）
・Facilitate x learning and BKM sharing for all related module related topics between global sites/HVM fabrications
・Assure that the right critical metric for inline param probe burn and REL measurements are in place assure appropriate reaction time for deviation and toggles
・Work with Yield Enhancement Process Engineering Real Time Defect Analysis Physical Failure Analysis Param and Quality Assurance teams to understand issues and priorities
・Pro actively address technical issues by proposing solutions and bring up resource conflicting.
・Take an ownership for across module activities and items in the critical path if required.
・Define sub milestones for the project and work with the team to achieve the targets and timelines
・Work with Central Teams Process areas and planning teams to define MOR related activities.
・Individual responsibilities
・Provide technical leadership for all of the related module activities for the lifetime of the project.
・Summarize a comprehensive problem derive and explain actions taken to address them.
・Drive effective multi functional communication on issue for resolution.

Required Skills

■Qualifications
・ 3 years of Process Integration or Process Development experience.
・Experience for the introduction and yield ramp for at least one DRAM generation.
・Capability to resolve an issue that span multiple groups.
・Ability to think and communicate clearly in urgent and stressed situations.
・Strong understanding of DRAM process flow as well as common Pareto issues.
・Understanding interaction of process and device.
・Previous exposure to transfer or production for at least one memory generation.
・Proficient communication skill in Japanese is a requirement.
・Well understanding of English will be a significant plus.
・Understanding of Chinese would be a plus.

■Education
Master of Science Degree in Electrical Engineering Microelectronics or related subject area is required （unless relevant multi year working expertise rationalizes waiving this requirement）

Company Description

ご紹介時にご案内いたします