CareerCross by JAC Recruitment

PR/157790 | Analog IC Design Manager

Job Information

Recruiter
JAC Recruitment Malaysia

Job ID
1512202

Industry
Other (Manufacturing)

Job Type
Permanent Full-time

Location
Malaysia

Salary
Negotiable, based on experience

Refreshed
December 24th, 2024 10:28

General Requirements

Minimum Experience Level
Over 3 years

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Business Level

Minimum Education Level
Associate Degree/Diploma

Visa Status
No permission to work in Japan required

Job Description

Analog IC Design Manager.

Rapidly expanding IC design platform company specialized in IP, SOC and ASIC design services hiring talented and experienced Analog Design Manager. You will part of large pool of well-trained engineers/designers who support customers in High-Performance Computing, AI, 5G & Network and Automotive industries using advanced technology.

Key Requirements of Analog IC Design Manager:

- Lead a team to complete the design and delivery of high-speed Serdes IPs
- Complete the design and simulation of analog circuits with proper design documentation
- Guide the layout / backend team to complete the physical implementation of IP and timing closure
- Assist in product testing, debugging and application
- Train junior analog designers on proper design and detailed documentation

Key Requirements:

- Master's degree or above in Microelectronics or Electronic Engineering, with more than 10 years of relevant work experience
- Have a solid understanding and experience in designing analog mixed signal circuit blocks, including bandgap, bias circuits, LDO regulators, amplifiers, comparators, switched capacitor circuits, ADCs, DACs, oscillators, filters, Tx/Rx

equalization techniques and circuits such as de-emphasis, CTLE, DFE, CDR architecture and implementation, high-speed digital circuits
- Have a deep understanding of analog mixed signal design, and experience in high-speed serial circuits using FinFET advanced technology
- Familiar with PCIe and other related protocols where familiarity with PCIe5 or PCIe6 is preferred
- Experience in developing 32G and above or PAM4 SerDes is preferred

Interested to explore this exciting opportunity? Apply below:

Company Description