



CYIENT

ASIC Digital Verification Engineer Lead

Job Information

Hiring Company

Cyient K.K.

Job ID

1490820

Industry

Electronics, Semiconductor

Company Type

Large Company (more than 300 employees)

Job Type

Permanent Full-time

Location

Kanagawa Prefecture

Salary

Negotiable, based on experience

Refreshed

November 19th, 2024 02:00

General Requirements

Minimum Experience Level

Over 6 years

Career Level

Mid Career

Minimum English Level

Business Level

Minimum Japanese Level

Business Level

N2 and above

Minimum Education Level

Bachelor's Degree

Visa Status

Permission to work in Japan required

Job Description

Position: ASIC Digital Verification Engineer Lead

Location: Yokohama

Language: N2 and above

Job Description:

Looking for 8+ yrs of design verification Engineers with below skills

- RTL design (Verilog HDL)
- EDA verification experience (NC Verilog)
- Ability to use Microsoft Office software (Excel, Word, Outlook)
- Ability to use Linux CUI commands

- Experience with SV, UVM and SystemVerilog Assertions (SVA)
- Experience using version control tools (Subversion, git)

Knowledge that would be beneficial

- AI Insights
- Ability to check timing reports during implementation

Roles & Responsibilities

- Under general supervision, performs engineering work and applied research, development, and design of new Integrated Chips.
- Work includes Architectural Design, Logic Design, Circuit Design, Physical Design, Verification, Fabrication, Packaging of Chips

Required Skills

Company Description