CareerCross

CYIENT

RTL設計・検証エンジニア/RTL Design and Verification Engineer

Job Information

Hiring Company
Cyient K.K.

Subsidiary
Cyient

Job ID
1444294

Industry
IT Consulting

Company Type
Small/Medium Company (300 employees or less) - International Company

Job Type
Permanent Full-time

Location
Tokyo - Other Areas

Salary
3 million yen ~ 7 million yen

Work Hours
9：00〜18：00（休憩1時間）　但し、弊社顧客プロジェクト対応の場合は顧客先営業カレンダーに準ずる

Holidays
土・日・祝　　但し、弊社顧客プロジェクト対応の場合は顧客先営業カレンダーに準ずる

Refreshed
July 8th, 2024 04:00

General Requirements

Minimum Experience Level
Over 3 years

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Business Level

Minimum Education Level
Bachelor's Degree

Visa Status
Permission to work in Japan required

Job Description

【業務内容】

・論理回路設計および検証業務（車載向けまたは産業用途向）

　タイミングチャートの記述および、要件仕様とりまとめ、回路ブロック図作成等をチームメンバーとして担当いただきます。

・その他付帯的業務

【応募条件】

必須条件

論理回路設計において、以下の経験をお持ちの方

- 機能要件をもとに、詳細なタイミングチャートの記述が可能
- 機能要件から詳細な仕様をまとめ、回路ブロック図を作成
- クロック同期を理解し、適正な同期回路を設計
- STARCルールを理解し、コーディングが可能
- ARM CPUやそのバス（AHB/AXI）の経験
- Linux OSの経験
- 検証項目から合否判定方法とその基準を定義

論理回路検証において、以下の経験をお持ちの方

- 検証項目の内容に従い、テストパターンを作成し、検証することが可能
- 信号が取り得る値や精度を定義し、各信号のビット幅を定義
- 最適な回路構成を定義するための数学的演算の拡張が可能
- FPGA/ASICのプリミティブを理解し、RAM校正や演算回路を設計可能
- 静的タイミング解析（STA）の基礎を理解

歓迎条件

- 技術系大学院卒業、4年以上の関連業務経験
- 日英バイリンガルで、記述や会話に優れている方
- **JLPT/NAT-TEST　資格保持者**

Key responsibilities:

Have the following experience in logic circuit design

- Able to describe detailed timing charts based on functional requirements.
- Formulate detailed specifications from functional requirements and create circuit block diagrams.
- Understanding clock synchronization and designing appropriate synchronization circuits
- Understand STARC rules and be able to code
- Experience on ARM CPU and/or its bus (AHB/AXI)
- Experience on Linux OS
- Define the pass/fail judgment method and its criteria from the verification items.

Have the following experience in logic circuit verification

- Test pattern can be created and verified according to the contents of the verification item
- Define the values and precision that signals can take and define the bit width of each signal.
- Expand mathematical operations to define the optimal circuit configuration
- Understand FPGA/ASIC primitives and design RAM configurations and arithmetic circuits
- Have a basic understanding of Static Timing Analysis (STA)

Desired Skills and Experience

- Technical Graduate with 4+ years of relevant experience
- Bilingual with good written and Verbal Communication
- **JLPT/NAT certified**

Company Description

About Cyient

Cyient is a global engineering and technology solutions company. As a Design, Build, and Maintain partner for leading organizations worldwide, we take solution ownership across the value chain to help clients focus on their core, innovate, and stay ahead of the curve. We leverage digital technologies, advanced analytics capabilities, and our domain knowledge and technical expertise, to solve complex business problems.

With over 15,000 employees globally, we partner with clients to operate as part of their extended team in ways that best suit their organization’s culture and requirements. Our industry focus includes aerospace and defence, healthcare, telecommunications, rail transportation, semiconductor, geospatial, industrial, and energy.